Claims:

1. A gold code generator comprising:

two pairs of linear feedback shift registers, wherein second seed values for the second pair of linear feedback shift registers are different from first seed values for the first pair of linear feedback shift registers, the second seed values being calculated from the first seed values, wherein the first and second pair of linear feedback shift registers are implemented to produce more than one new state bit and more than one output bit for each linear feedback shift registers at the same time.

2. The gold code generator of claim 1 wherein the seed values for the second pair of linear feedback shift registers are delayed values of the first seed values.

3. The gold code generator of claim 1 wherein the gold code generator is implemented on a reconfigurable logic chip.

4. The gold code generator of claim 3 wherein the calculation of some of the second seed values is done using a dedicated processor on the reconfigurable chip.

5. The gold code generator of claim 3 wherein the gold code generator configuration is loaded into a background plane of the reconfigurable chip, while the reconfigurable chip is operating on another configuration in the foreground.

6. The gold code generator of claim 3 wherein the feedback is implemented using lookup tables.

7. A system comprising:

at least one reconfigurable chip implementing a gold code generator, the at least one reconfigurable chip including background and foreground configuration memories, wherein the background configuration memory is adapted such that it can be loaded with a gold code generator configuration while the at least one reconfigurable chip, configured with the foreground plane, operates, and wherein after the background configuration loads, the gold code generator configuration can be activated to reconfigure the at least one reconfigurable chip.

8. The system of claim 7 wherein the gold code generator comprises two pairs of linear feedback shift registers wherein the seed values for the second pair of linear feedback shift registers is different from the seed values for the first pair of linear feedback shift registers.

9. The gold code generator of claim 7 wherein the second seed values are calculated from the first seed values.

10. The gold code generator of claim 9 wherein the calculation of the second seed values is done at least partially in a processor on the reconfigurable chip.

11. The system of claim 10 in which the gold code generator is implemented to produce more than one output bit at the same time.

12. A method of implementing a pseudo-random code generator:

converting a pseudo-random code generator specification into an equivalent representation, the pseudo-random code generator specification being such that taps used to calculate an output include at least one tap within n spaces from the

input, the equivalent representation is such that no such taps are within n spaces from the input; and

implementing the equivalent representation such that multiple new state bits are calculated at the same time.

13. The method of claim 12 wherein the pseudo-random code generator specification being such that taps to calculate an output is defined within a first chip register span, the equivalent representation is such that taps to calculate an output bit are within a smaller shift register span.

14. The method of claim 12 wherein the equivalent representation includes two pairs of linear feedback shift registers wherein the second seed values for the second pair of linear feedback shift registers is different from a first seed value for the first pair of linear feedback shift registers.

15. The method of claim 12 wherein the pseudo-random code generator comprises a gold code generator.

16. The method of claim 12 wherein the pseudo-random code generator is implemented on a reconfigurable chip.

17. A method of implementing a pseudo-random code generator comprising:

converting a pseudo-random code generator specification into an equivalent representation, the pseudo-random code generator specification being such that taps to calculate an output are defined within a first shift register span, the equivalent representation is such that the taps to calculate an output bit are within a smaller shift register span; and

implementing the equivalent representation such that multiple output bits are calculated at the same time.

18. The method of claim 17 wherein the pseudo-random code generation specification is such that taps used to calculate an output have at least one tap within *n* spaces from the input, the equivalent representation is such that no such tap is within *n* spaces from the input.

19. The method of claim 17 wherein two pairs of linear feedback shift registers are used in the equivalent representation.

20. The method of claim 19 wherein the second seed values for the second pair of linear feedback shift registers are different from the first seed values for the first pair of linear feedback shift registers.

21. The method of claim 17 implemented on a reconfigurable chip.

22. The method of claim 17 wherein in the equivalent representation of the output bits are calculated from taps at a single register for each linear feedback shift register.